IN THE SPECIFICATION

Please amend the specification as follows:

On page 6, line 12, please change "plurality of flip-flops" to --plurality of flip-flops 762 to 766-- as shown below:

The first data align signal generator 260 has a plurality of flip-flops 762 to 766. Each flip-flop receives each delayed rising DLL clock, e.g., RCLK_DLL_OE1, RCLK_DLL_OE2 and RCLK_DLL_OE3 and the rising DLL clock RCLK_DLL at a clock terminal and outputs each data align signal, e.g., SOSEZ15, SOSEZ25, SOSEZ35, SOSEZ45 and SOSEZ55. Likewise, if not shown, the second data align signal generator 270 has a plurality flip-flops which respectively receive each delayed falling DLL clock, e.g., FCLK_DLL_OE1, FCLK_DLL_OE2 and FCLK_DLL_OE3 and the falling DLL clock FCLK_DLL at a clock terminal and outputs each data align signal.

On page 11, line 7, please change "signal generator" to --signal generator 930-- as shown below:

The domain crossing circuit includes a domain crossing sensing block 920, a first output enable signal generator 910, a second output enable signal generator 930, a data controller 940, a data output controller 950, a first data align signal generator 960 and a second data align signal generator 970.

On page 13, line 19, please change "MUX 431" to --MUX 1231-- as shown below:

The internal to DLL phase detection block has first to third flip-flops 1211 to 1213 and a first MUX ~~431~~1231. The first flip-flop 1211 synchronizes the supply voltage VDD with the internal clock INT_CLK, and the second and third flip-flops 1212 and 1213 respectively synchronizes an outputted signal of the first flip-flop with the rising and falling DLL clock FCLK_DLL and RCLK_DLL.

On page 13, line 28, please change "MUX 431" to --MUX 1231-- as shown below:

Thereafter, the first MUX ~~431~~ 1231 included in the internal to DLL phase detection block selects one of the outputted signals F and R of the second and third flip-flops 1212 and 1213 in response to the setup selection signal SELB.

On page 14, line 1, please change "MUX 431" to --MUX 1231-- as shown below:

Next, in latency detection start block 1241, the selected signal OE01 outputted from the first MUX ~~431~~ 1231 is synchronized with the rising DLL clock RCLK_DLL. The latency detection start block 1241 outputs the phase detection signal FPVT_DET.